Multilevel level single phase inverter implementation for reduced harmonic contents

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ABSTRACT

Selective harmonic elimination technique SHE is adopted in this work to reduce the harmonic contents in single phase cascaded multilevel inverter. The firing instants for the electronic switches MOSFETs in the inverter are calculated off line for five level to thirteen level inverter. An Arduino microcontroller is programmed to cope with different topologies of the multilevel inverter. The implemented multi-level (MLI) inverter results are compared with Simulink simulation program and are found very close to each other. SHE technique works at system frequency (50 Hz or 60 Hz) and the switching losses are very small. The sinusoidal pulse width modulation SPWM requires a carrier frequency not less 20 times the system frequency so SHE approach is found to be superior compared with SPWM. Also, SHE technique shows significant reduction in THD as the number of levels increased. Results for the output voltages and currents along with their frequency spectrum are shown and compared with traditional SPWM.

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1. INTRODUCTION

Multilevel inverters consist of cascaded stages of single-phase inverters. They are used for high power conversion from DC to AC. They found wide range of applications in transport, electric vehicles, renewable energy and many other applications [1]. Multilevel inverters have two distinct features. First, they operate at system frequency (low order 50 Hz or 60 Hz) which means very low switching losses. Second the output voltage has very low total harmonic distortion due to the multi stair shape in the output. The cascaded multilevel inverters CMLI is designed by using H-bridges in series and its arrangement is simple, the most attractive of this topology in the medium to high voltage (2-13 Kv) [2]. ther types of inverter like Neutral point clamped (NPC) inverters and flying capacitor (FC) inverters. Main disadvantage of CMLI configuration is the increase number of switching devices and its complex driver circuit [3]. By developing new topology of inverters, the complexity can be reduced and hence the reliability can be increased. By having inverters with a smaller number of switches, for the similar voltage level the reliability of the inverters can be improved [4]. Most recently the CML inverters are used in the field of renewable energy [5]. Recent development of CML includes low switching frequency based asymmetrical multilevel inverter topology with reduced switch count [6] and A new multilevel inverter topology with reduce switch count [7]. In this work CML with two, three and four H-bridges four controlled by Arduino microcontroller is implemented. A Simulink model for selective harmonic elimination is built through Matlab and the results are compared with the practical ones. Then these results are compared with the traditional sinusoidal pulse modulation technique

to verify the validity of the proposed model. The control of the inverter output voltage is important for many aspects like the variation of the input dc voltage, to get a regulated output voltage and to keep the voltage to frequency ratio at constant mode [6]. The inverter gain can be controlled in different techniques employing PWM control as the basic building block. The sinusoidal PWM is commonly used where a sinusoidal reference signal with a frequency f_r is compared with a triangular carrier wave of frequency f_c . In this method f_c is in kilohertz range compared with low frequency f_r i.e. 50 Hz or 60 Hz. The MOSFEs, which are commonly used as electronic switches in the inverter topology, must be chosen to cope with the carrier frequency, which results in significant high-power loss. The alternative method is to use selective harmonic elimination method SHE where the inverter works only on the reference signal frequency f_r. The instantaneous output voltage of the inverter is a square wave with f_r frequency (i.e. 50 Hz or 60 Hz). This voltage can be expressed in Fourier series as

$$v_o = \frac{a_o}{2} + \sum_{n=1}^{\infty}(a_n \cos(nwt) + b_n \sin(nwt)) \tag{1}$$

Due to quarter wave symmetry along the x-axis, both a_o and a_n are zero. We get

$$b_{n=} \frac{1}{\pi}\left[\int_{\frac{-\pi}{2}}^{0}\frac{-V_s}{2}\sin(nwt)\,d(wt) + \int_{0}^{\frac{\pi}{2}}\frac{V_s}{2}\sin(nwt)\,d(wt)\right] = \frac{2V_s}{n\pi} \tag{2}$$

Which gives the instantaneous output voltage

$$\begin{aligned} v_o &= \sum_{n=1,3,5,\ldots.}\frac{2V_s}{n\pi}\sin(nwt) \\ &= 0 \text{ for } n = 2,4,6 \end{aligned} \tag{3}$$

For the unipolar output voltage notches the coefficient b_n is given by

$$b_{n=} \frac{4V_s}{\pi}\left[\int_{0}^{\alpha_1}\sin(nwt)\,d(wt) + \int_{\alpha_2}^{\frac{\pi}{2}}\sin(nwt)\,d(wt)\right] = \frac{4V_s}{\pi}\frac{1-\cos n\alpha_1+\cos n\alpha_2}{n} \tag{4}$$

In (4) can be extended to m notches per quarter wave (quasi-square symmetry) as,

$$b_n = \frac{4V_s}{n\pi}\left[1 + \sum_{k=1}^{m}(-1)^k\cos(n\alpha_k)\right] \text{ for } n = 1,3,5, \tag{5}$$

where $\alpha_1 < \alpha_2 < \cdots .. \alpha_k < \frac{\pi}{2}$

This method works efficiently for any number of harmonics to be eliminated and adopted throughout this work. Multilevel inverters include an array of power semiconductor switches especially MOSFET's and a combination of DC sources, the output of multilevel inverter is stepped waveforms of theses DC sources. If we let s as the number of steps of the phase voltage with reference to the negative terminal of the inverter, then the number of steps in the voltage between the two phases of the load k is $k = 2s + 1$. The total harmonic distortion (THD) can be reduced significantly if we increase the number of levels in the inverter. The efficient control methods for multilevel inverters may include sinusoidal pulse width modulation (SPWM), space vector pulse width modulation (SVPWM) and selective harmonic elimination [7].

2. SELECTIVE HARMONIC ELIMINATION

In this technique, numbers of harmonics to be eliminated is to be defined. For instance, a seven-level inverter, we have three full bridge inverter then the 3rd, 5th harmonics are to be eliminated. An off-line determination for the switching instants of the multilevel inverter is shown in Figure 1. After locating α_1, α_2 and α_3 on the Figure a mirror image is drawn around $\pi/2$, this is what we need for the positive cycle of the inverter output. Then the process is repeated for the negative output cycle. These instants are fed to the MOSFET switches according to each level and the expected output voltage is shown in Figure 2. Table 1 and Figure 3 summarizes the MOSFET switches state, the period of operation and the level of the output voltage for a seven level MLI. The following nonlinear equations has to be solved in order to find the values for the triggering anglesα_1, α_2 and α_3.

$$1 - \cos\alpha_1 + \cos\alpha_2 - \cos\alpha_3 = \frac{4V_s}{\pi} \tag{6}$$

$$1 - \cos 3\alpha_1 + \cos 3\alpha_2 - \cos 3\alpha_3 = 0 \quad (7)$$

$$1 - \cos 5\alpha_1 + \cos 5\alpha_2 - \cos 5\alpha_3 = 0 \quad (8)$$

A Newton Raphson method is used as a common numerical solver for nonlinear solution, which determines the values to be: $\alpha_1 = 13.22\,°, \alpha_2 = 38°$ and $\alpha_3 = 82.9°$.

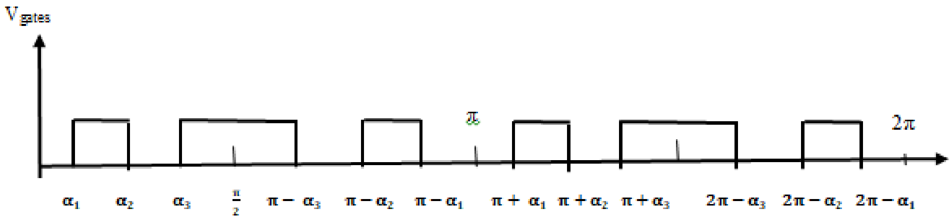


Figure 1. Determination of triggering instants using quarter wave symmetry

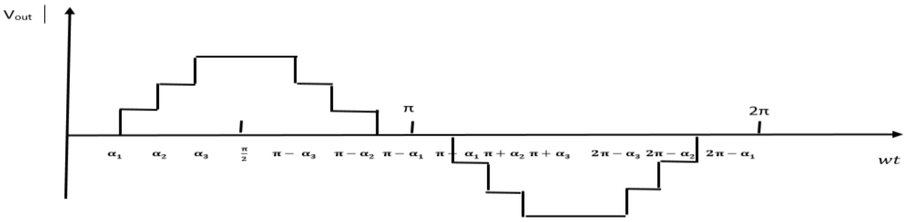


Figure 2. The expected output voltage for Figure 1

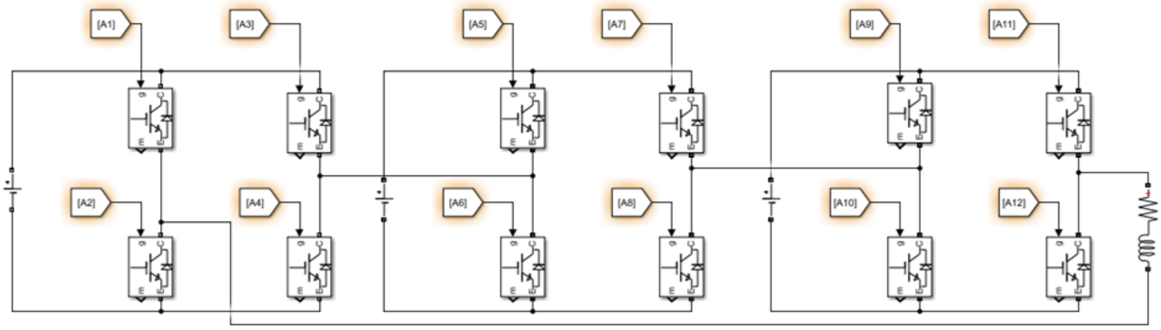


Figure 3. Seven level inverter

Table 1. Determination of triggering instants for seven level MLI inverter

S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	Period	DC level
1	0	1	0	1	0	1	0	1	0	1	0	α_1	0
1	1	0	0	1	0	1	0	1	0	1	0	$\alpha_2 - \alpha_1$	$+V_{DC}$
1	1	0	0	1	1	0	0	1	0	1	0	$\alpha_3 - \alpha_2$	$+2V_{DC}$
1	1	0	0	1	1	0	0	1	1	0	0	$\pi - 2\alpha_3$	$+3V_{DC}$
1	1	0	0	1	1	0	0	0	1	0	1	$\alpha_3 - \alpha_2$	$+2V_{DC}$
1	1	0	0	0	1	0	1	0	1	0	1	$\alpha_2 - \alpha_1$	$+V_{DC}$
0	1	0	1	0	1	0	1	0	1	0	1	$2\alpha_1$	0
0	0	1	1	0	1	0	1	0	1	0	1	$\alpha_2 - \alpha_1$	$-V_{DC}$
0	0	1	1	0	0	1	1	0	1	0	1	$\alpha_3 - \alpha_2$	$-2V_{DC}$
0	0	1	1	0	0	1	1	0	0	1	1	$\pi - 2\alpha_3$	$-3V_{DC}$
0	0	1	1	0	0	1	1	1	0	1	0	$\alpha_3 - \alpha_2$	$-2V_{DC}$
0	0	1	1	1	0	1	0	1	0	1	0	$\alpha_2 - \alpha_1$	$-V_{DC}$
1	0	1	0	1	0	1	0	1	0	1	0	α_1	0

3. IMPLEMENTATION OF MULTILEVEL SINGLE-PHASE INVERTER

Ersoy Beser presents a single-phase multilevel inverter for using as a voltage harmonic source. The switching signals are determined by a PIC18F45 microcomputer [8]. Tapan Kumar addresses the simulation and practical implementation of a single –phase multilevel inverters consisting of three H-bridge units to generate a maximum of 14 level output voltage. the set signals for MOSFETs are generated by using ATmega 2560 micro controller-based Arduino board [9]. Pouya Tarassadi paper introduces a SPWM cascaded full bridge single phase 7-level inverter with optimized shift modulation [10]. In this work implementation of cascaded multilevel inverter for variety of unlimited levels. The triggering instants are generated by ATmega 2560. The strategy of triggering angles is based on selective harmonic elimination. In this case the operating frequency is the system frequency i.e. 50 Hz or 60 Hz. No need for any high carrier frequency as the case in SPWM. Then a Simulink model is built, and results are compared with practical ones for validation. A prototype model for cascaded multilevel inverter consists of power section of four single phase inverter that is 16 MOSFETs for switching purpose. The controller is Arduino Mega 2560 with 16 digital output signals. Four optocouplers are used to isolate the controller and the power circuit from any abnormal working conditions. For any level of the cascaded MLI associated off line program is uploaded to the controller and the related triggering instants are fed to the MOSFETs. The practical results are compared with a Simulink model built for this purpose. Generation of any multilevel output voltage from single-phase multilevel inverter consisting of cascaded three H-bridge units [11]-[17]. A New multilevel level single-phase inverter employing vector control gives better utilization of dc power supply and reduced harmonic distortion [18-20]. Adopting Low switching frequency control reduces power losses and enhancing the THD factor in the multilevel cascaded H bridge inverters [21]-[27].

4. RESULTS

Two cascaded single-phase H bridge inverter are connected to get five level inverter. Two nonlinear equations are solved using Newton Raphson method and the triggering angles are determined to be $\alpha_1 = 5.07° \; and \; \alpha_2 = 54.9°$. Figure 4(a) shows the output voltage for five level inverter with two dc power supply 10V each (max output=20V) and for modulation index m=1. The output current for the five-level inverter with inductive load with $R = 5\Omega \; and \; L = 5mH$ is shown in Figure 4(b). The frequency spectrum shows the absence of the 3rd . The 5th harmonics is present at 250 Hz followed by the 7th harmonics at 350 Hz.The current starts a new value according to the triggering instants. Here we have two distinct change of current as we have two triggering instants.

$$1 - \cos\alpha_1 + \cos\alpha_2 = \frac{4V_s}{\pi} \tag{9}$$

$$1 - \cos 3\alpha_1 + \cos 3\alpha_2 = 0 \tag{10}$$

(a) (b)

Figure 4. (a) five level inverter shows the output voltage and frequency spectrum 156.25 Hz/div, (b) output current

For a seven-level inverter (with three dc power supply 10V each ,max output=30V) and for modulation index m=1 There are seven different values of output voltage, manly 0Volt, $+V_{DC}$, $+2V_{DC}$,

$+3V_{DC}$, $-V_{DC}$, $-2V_{DC}$ and $-3V_{DC}$, where V_{DC} is the DC input to the inverter. Here we have three nonlinear equations to be solved.

$$1 - \cos\alpha_1 + \cos\alpha_2 - \cos\alpha_3 = \frac{4V_s}{\pi} \tag{11}$$

$$1 - \cos3\alpha_1 + \cos3\alpha_2 - \cos3\alpha_3 = 0 \tag{12}$$

$$1 - \cos5\alpha_1 + \cos5\alpha_2 - \cos5\alpha_3 = 0 \tag{13}$$

The values of the triggering angles are found to be $\alpha_1 = 13.22\,°, \alpha_2 = 38°\ and\ \alpha_3 = 82.9°$.

The output voltage along with its frequncy spctrum is shown in Figure 5(a). The frequency spectrum shows the absence of the 3rd and 5th harmonics. The 7th harmonic is present at frequency = 350 Hz. Here we have three different instants of triggering and so we have three different changes in the current values as shown in Figure 5(b). This makes the current approaches more sinusoidal shape, which in turns reduces the total harmonic distortion THD.

(a) (b)

Figure 5. Seven level inverter (a) output voltage and frequency spectrum 156.25 Hz/div (b) output current

As we increase number of inverter levels more odd harmonics is eliminated and the shape of the out current approaches more sinusoidal shapes. This is clear in the nine-level inverter shown in Figure 6(a) where the 3rd,5th and 7th harmonics are eliminated. Frequency spectrum shows the presence of the 9th harmonic at frequency =450 Hz. The output current is shown in Figure 6(b). Here we have five nonlinear equations to be solved

$$1 - \cos\alpha_1 + \cos\alpha_2 - \cos\alpha_3 + \cos\alpha_4 = \frac{4V_s}{\pi} \tag{14}$$

$$1 - \cos3\alpha_1 + \cos3\alpha_2 - \cos3\alpha_3 + \cos3\alpha_4 = 0 \tag{15}$$

$$1 - \cos5\alpha_1 + \cos5\alpha_2 - \cos5\alpha_3 + \cos5\alpha_4 = 0 \tag{16}$$

$$1 - \cos7\alpha_1 + \cos5\alpha_2 - \cos7\alpha_3 + \cos7\alpha_4 = 0 \tag{17}$$

And the corresponding solution gives $\alpha_1 = 5.25°, \alpha_2 = 28.12°\,, \alpha_3 = 46.38°\ and\ \alpha_4 =\ 84.09°$.

A practical set for multilevel single-phase inverter that is used for different cascaded MLI is shown in Figure 7. As the number of levels is increased the THD is decreased significantly as conclude in Table 2.

A proteus program for a nine level inverter that is uploaded to the ardunio microcontroller and shown in Figure 8(a). A Matlab file for calculating the triggering angles for nine level inverter is shown in Figure 8(b). To ensure quarter wave symmetry $\alpha_1 < \alpha_2 < \alpha_3 < \alpha_4 < \alpha_5 < \pi/2$. In order to work with different values of modulation indexes $(0 < m < 1)$ an m file is executed and the relation between the modulation index and its corresponding triggering angles is shown in Figure 8(c).

(a) (b)

Figure 6. Nine level inverter (a) voltage and frequency spectrum 156.25 Hz/div (b) output current

Figure 7. A practical set for MLI

Table 2. THD values for different inverter levels

No. of levels	Fundamental	THD
five	20.03%	27.03%
Seven	29.94%	17.92%
Nine	35.88%	14.95%
Eleven	49.9%	10.53%

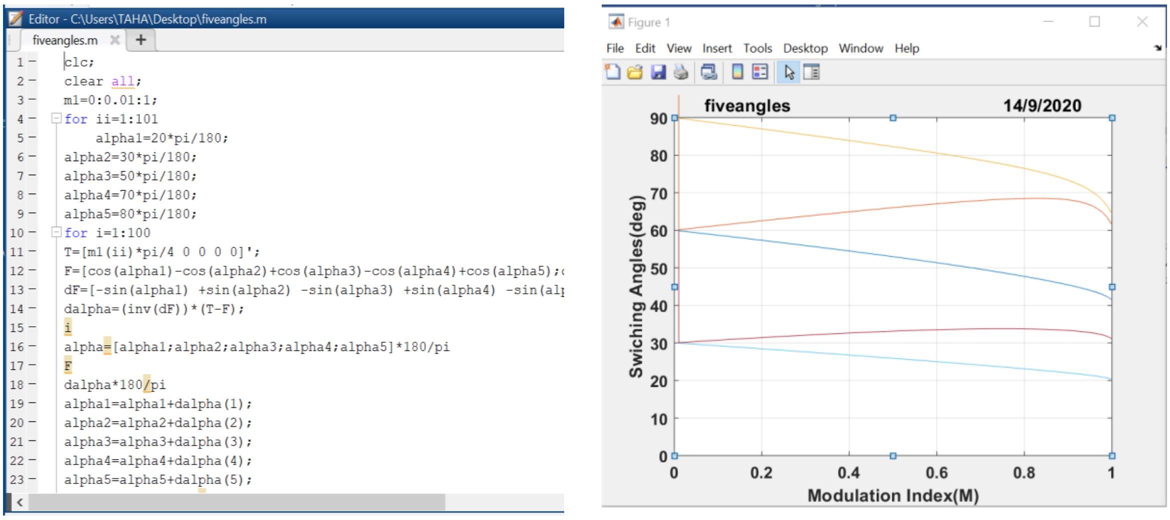
ninelevelshe | Arduino 1.8.9

File Edit Sketch Tools Help

ninelevelshe §

```
//alphal =5.2538  alpha2=28.1201 alpha3=46.3876  alpha4=84.0986  alphal=(5.2538/360)*20 000=291.8777
float alphal = 291.8777;
float alpha2 = 1562.2277;
float alpha3 = 2577.0888;
float alpha4 = 4672.1444;
float pi = 10000.0;
int Sl=1; int S2=2; int S3=3; int S4=4; int S5=5; int S6=6; int S7=7; int S8=8;
int S9=9; int S10=10; int S11=11; int S12=12; int S13=13; int S14=14; int S15=15; int S16=16;
void setup() {  pinMode (S1, OUTPUT);pinMode (S2, OUTPUT); pinMode (S3, OUTPUT); pinMode (S4, OUTPUT);
                pinMode (S5, OUTPUT);pinMode (S6, OUTPUT); pinMode (S7, OUTPUT); pinMode (S8, OUTPUT);
                pinMode (S9, OUTPUT);pinMode (S10, OUTPUT); pinMode (S11, OUTPUT); pinMode (S12, OUTPUT);
                pinMode (S13, OUTPUT);pinMode (S14, OUTPUT); pinMode (S15, OUTPUT); pinMode (S16, OUTPUT);  }
void loop() {
//-------------------- 1 --------------------//
digitalWrite (S1 , HIGH); digitalWrite (S2 , LOW); digitalWrite (S3 , HIGH); digitalWrite (S4 , LOW);
digitalWrite (S5 , HIGH); digitalWrite (S6 , LOW); digitalWrite (S7 , HIGH); digitalWrite (S8 , LOW);
digitalWrite (S9 , HIGH); digitalWrite (S10 , LOW); digitalWrite (S11 , HIGH); digitalWrite (S12 , LOW);
digitalWrite (S13 , HIGH); digitalWrite (S14 , LOW); digitalWrite (S15 , HIGH); digitalWrite (S16 , LOW);
delayMicroseconds (alphal);
////-------------------- 2 --------------------//
digitalWrite (S2 , HIGH); digitalWrite (S3 , LOW); delayMicroseconds (alpha2 - alphal);
////-------------------- 3 --------------------//
digitalWrite (S6 , HIGH); digitalWrite (S7 , LOW); delayMicroseconds (alpha3 - alpha2);
////-------------------- 4 --------------------//
digitalWrite (S10 , HIGH); digitalWrite (S11 , LOW); delayMicroseconds (alpha4 - alpha3);
////-------------------- 5 --------------------//
digitalWrite (S14 , HIGH); digitalWrite (S15, LOW); delayMicroseconds (pi - (2*alpha4));
////-------------------- 6 --------------------//
digitalWrite (S13 , LOW); digitalWrite (S16 , HIGH); delayMicroseconds (alpha4 - alpha3);
////-------------------- 7 --------------------//
digitalWrite (S9 , LOW); digitalWrite (S12 , HIGH); delayMicroseconds (alpha3 - alpha2);
////-------------------- 8 --------------------//
digitalWrite (S5 , LOW); digitalWrite (S8 , HIGH); delayMicroseconds (alpha2 - alphal);
////-------------------- 9 --------------------//
digitalWrite (S1 , LOW); digitalWrite (S4 , HIGH); delayMicroseconds (2*alphal);
////-------------------- 10 --------------------//
digitalWrite (S2 , LOW); digitalWrite (S3 , HIGH); delayMicroseconds (alpha2 - alphal);
////-------------------- 11 --------------------//
digitalWrite (S6 , LOW); digitalWrite (S7 , HIGH); delayMicroseconds (alpha3 - alpha2);
```

(a)



(b) (c)

Figure 8. Illustrating programmes (a) proteus program, (b) M-file Neton Raphson, (c) modulation index range

The Simulink model for nine level MLI using selective harmonic approach (with the same DC supply voltages values that are used in the practical part i.e. 10V/supply is shown in Figure 9. The output voltage shown in Figure 10 shows agreement compared with the practical results shown previously in Figure 6 and the THD value is within the accepted level.

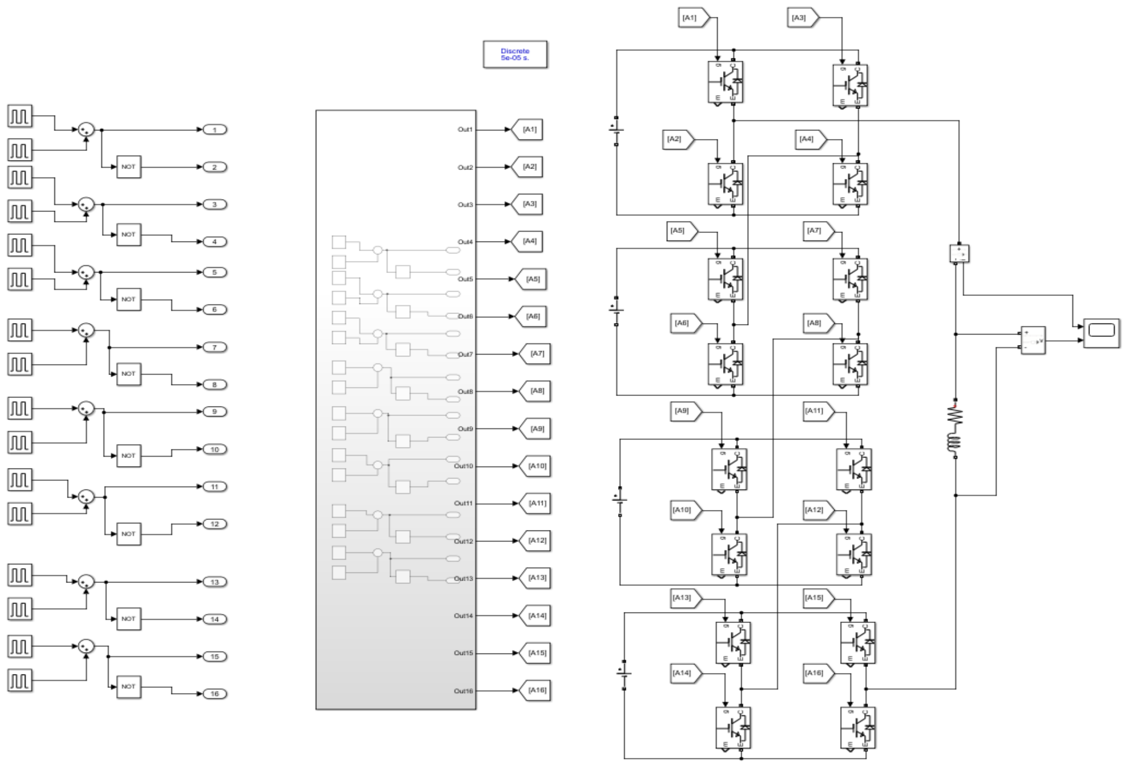


Figure 9. Matlab Simulink model for nine level inverter using SHE

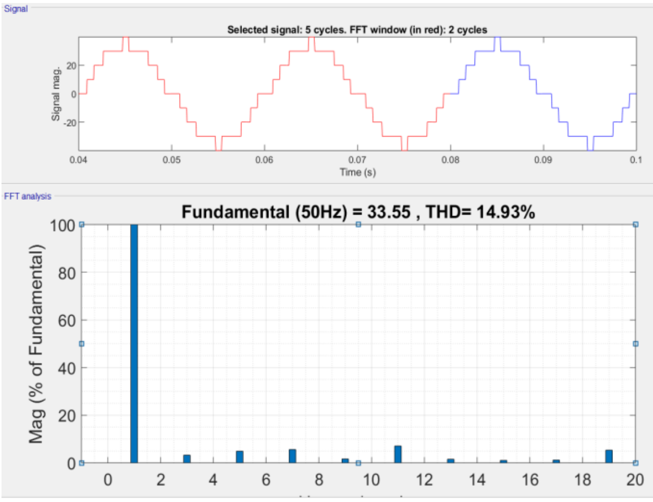


Figure 10. Simulink output voltage and frequency spectrum for nine level inverter using SHE

To compare SHE technique with SPWM a Simulink model for nine level MLI using SPWM approach is shown in Figure 11. A carrier frequency of $f_c = 1300Hz$ is used for the triangular waveform supply.

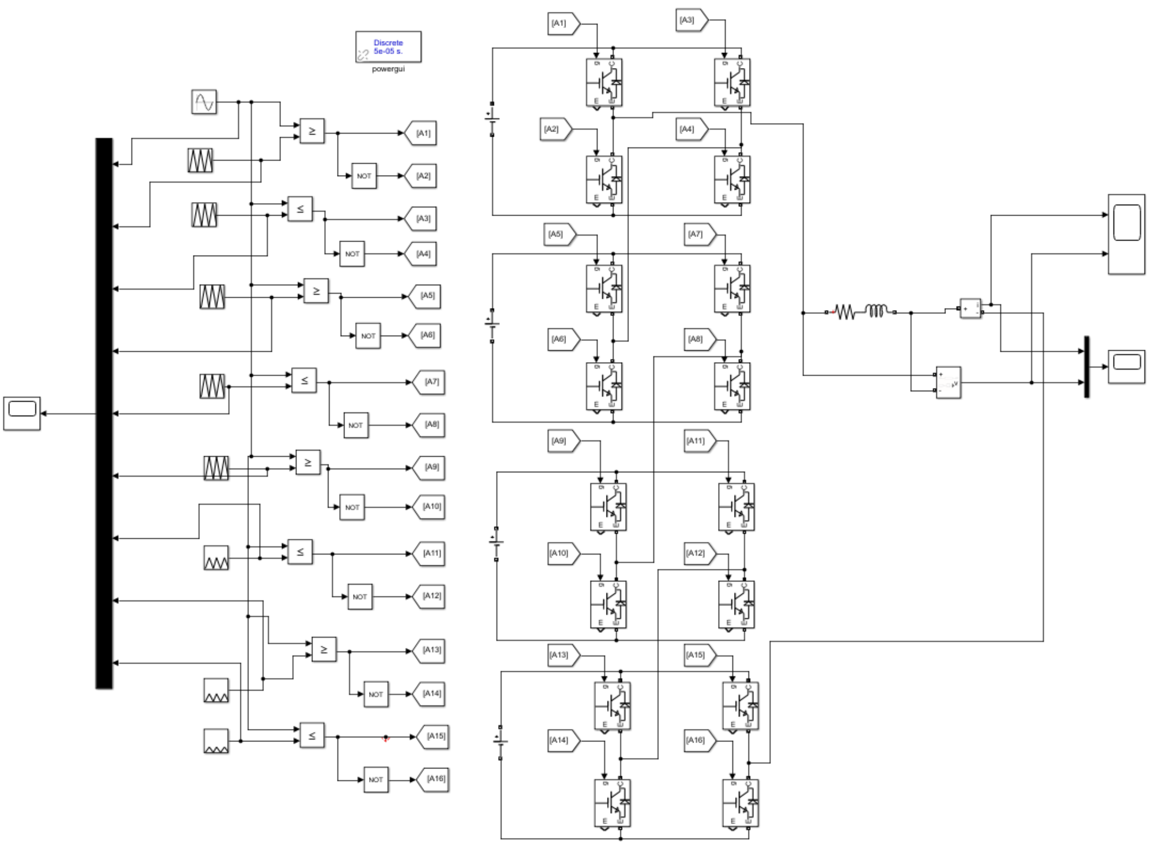


Figure 11. Matlab Simulink model for nine level inverter using SPWM

Eight equal levels of triangular waves with $f_c = 1300Hz$ are needed to cross the sinusoidal system frequency $f = 50Hz$ shown in Figure 12 and the triggering instants are defined.

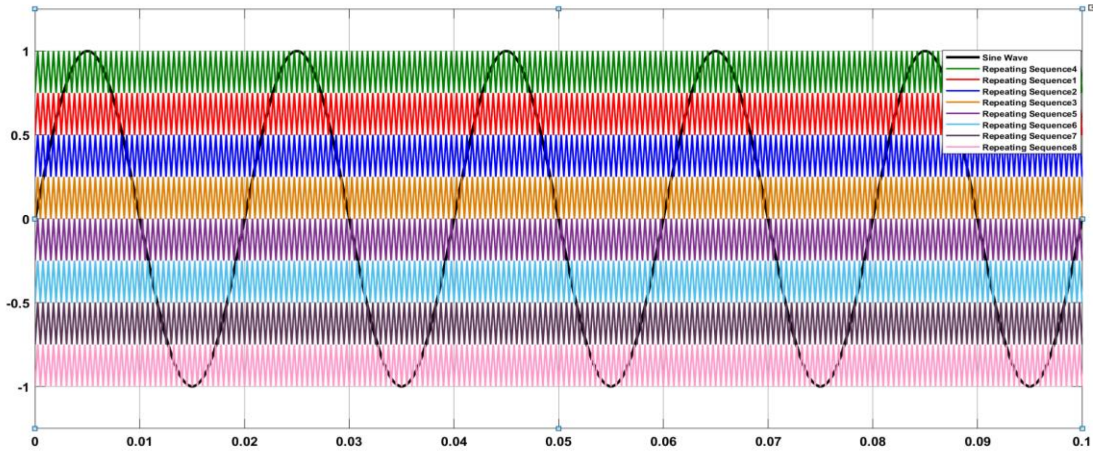


Figure 12. Sinusoidal pulse width modulation criteria for nine level inverter

The output voltage with its frequency spectrum is shown in Figure 13 and are almost similar to the output shown in Figure 10 for SHE technique. Due to high carrier frequency the number of triggering instants in SPWM are very large compared with the limited triggering instants in SHE approaches. This will increase the switching losses compared with SHE technique.

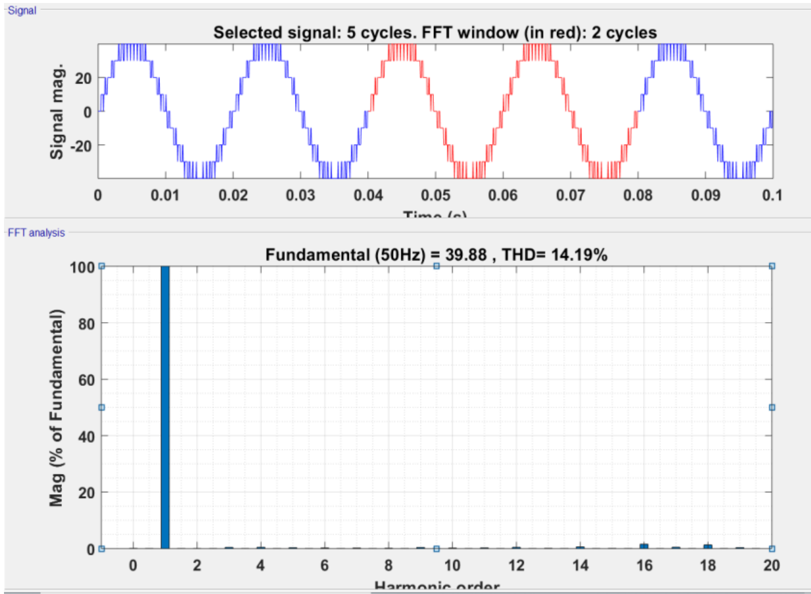


Figure 13. Simulink output voltage and frequency spectrum for nine level inverter using SPWM

This makes SHE technique the preferable method to be used in inverter applications. Recently many works were done to decrease number of switching devices in order to decrease the switching losses [4]. A modified Simulink model shown in Figure 14. To the centre of the left diode bridges a MOSFET transistor is added that will allow to change the path of the current in a sequence to eliminate some of switches needed in MLI. For example, to get 13 level MLI we need 6 H-bridges, but the mentioned topology reduces the number of H-bridges to three only with addition of three controlling MOSFETs transistors. This approach can be used in all previous topologies. The Simulink output current and voltage are shown in Figure 15 and the staircase of the thirteen levels are very smooth.

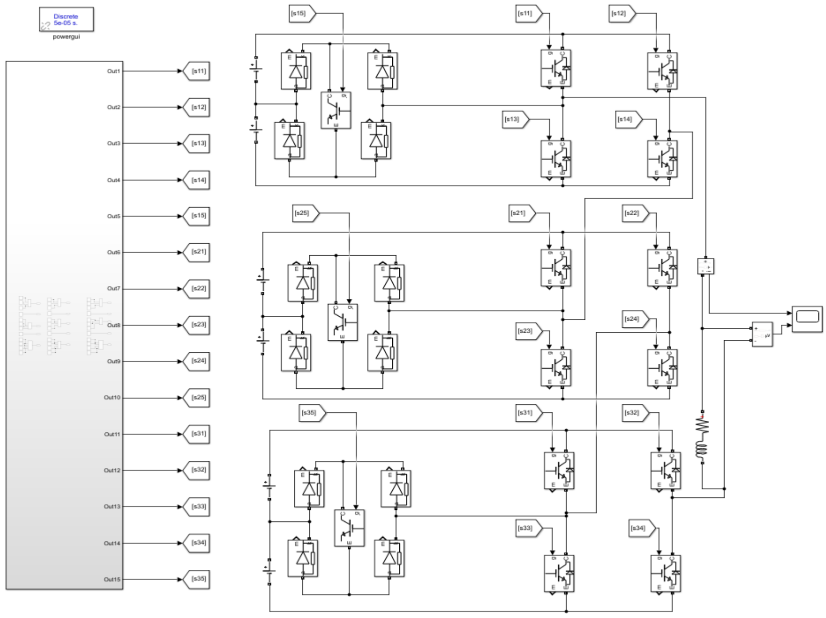


Figure 14. Modified Simulink model for eleven level inverter using SHE

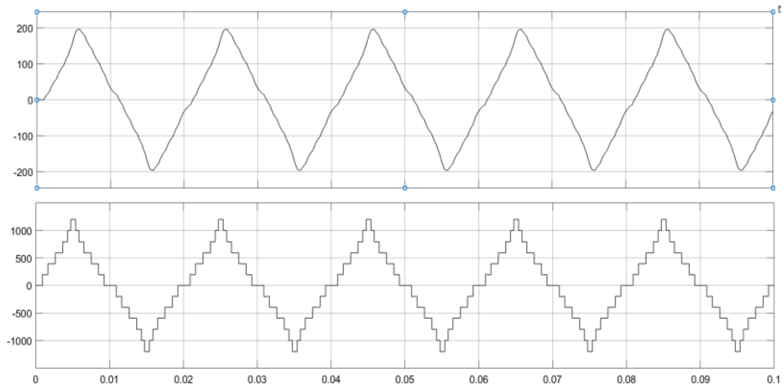


Figure 15. Simulink output current and voltage for thirteen levels MLI

5. CONCLUSION

Implementation of cascaded multilevel single-phase inverter using selective harmonic elimination approach shows reduced total harmonic distortion THD and few hard ware components compared with the traditional sinusoidal pulse width modulation SPWM. The implementation ensures any desired level ranges starting from five level inverter. The triggering instants for the operation of the MOSFETs switches are determined when solving the related nonlinear sinusoidal equations using the traditional Newton Raphson method. Arduino Mega 2560 microcontroller is used for the generation of the digital signals and injected to the gates of the MOSFETs. An optocoupler insulator is added between the inverter circuit and the microcontroller to ensure safety operation of both hardware's. The practical results show agreement with the Simulink model in Matlab software for the cases studied in this work. A Simulink for a recent modified multilevel inverter topology that reduces the number of the H-bridge is also shown for thirteen level inverter and it is suggested to be implemented in future work.

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